Characterization of Micro-Bumps for 3DIC Wafer Acceptance Tests

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***Abstract*—The strong market needs to embed multiple functionalities from different semiconductor processing technologies into a single system continue to drive demands for more advanced 3DIC packaging technologies. Dimensions of copper pillar micro-bumps are consistently reduced in every new technology node to facilitate the 3D stacking of multiple dies so that overall system performance can be improved. Semiconductor packaging companies must perform wafer acceptance tests to qualify their copper pillar micro-bumping process. Probecards and single DC probes are unable to address the measurement challenges and flexibilities needed for micro-bump wafer acceptance tests, which measure the micro-bump resistance and the wafer surface leakage currents in a single setup. In this paper, consistent and repeatable test results are obtained in a fully automatic manner using custom DC positioners with theta-X planarizing capability and true Kelvin probes for micro-bump resistance measurements as well as standard DC probes for wafer surface leakage measurements.**

Keywords—3DIC, micro-bumps, bumps, daisy-chain, 4-point Kelvin, Kelvin, resistance, wafer surface leakage measurements, wafer acceptance tests, WAT, and IC packaging.

I. Introduction

Packaging multiple integrated circuit dies together in a 3D stacking approach to form the whole system or product has greatly improve product performance and flexibility while reducing production costs [1]. Such packaging approach allows circuit designers to optimize the speed of their integrated circuits through vertical routing and reduction of RLC parasitic delay, especially for critical clock signal in the system. In addition to performance improvements, with 3D IC stacking, products now can accommodate for more functionalities through heterogenous stacking of different semiconductor technologies, that have specific performance merits, such as compound semiconductor devices onto CMOS logic silicon substrate, resulting in both better performance and a much smaller form factor for the final product.

To fabricate 3D IC packaging or stacking, semiconductor foundries and packaging companies have developed silicon interposers with redistribution layers, copper pillars and micro-bumps. These allow for the mechanical and electrical integration of multiple dies which could be fabricated with different semiconductor processing technologies for various functionalities. The performance of these micro-bumps and interposers are ensured by measuring the resistance of the micro-bumps as well as characterizing wafer surface leakage current as wafer acceptance tests prior to forming the 2.5D or 3D IC die stack. With the continual reduction of the bump diameter as shown in Figure 1, it is getting more challenging and very difficult to accurately and repeatably characterize the performance these micro-bumps efficiently. This paper discusses the challenges and presents a viable solution to characterize the performance of the micro-bump process in a fully automatic fashion for production tests.

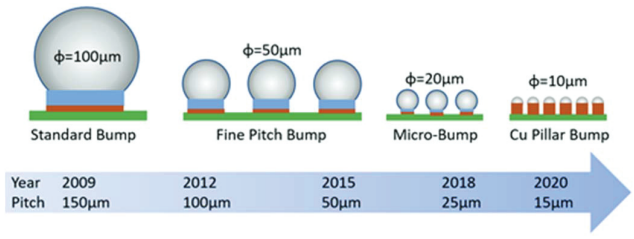
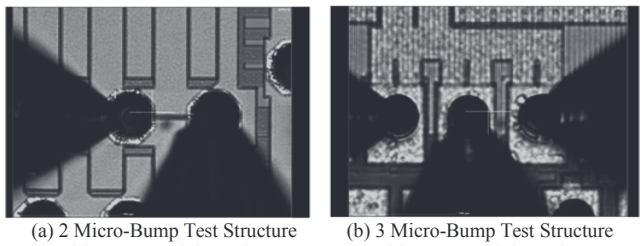


Fig. 1. Bump Technology Roadmap.

II. Test Structure Design and Experimental Setup

Dedicated daisy-chain and 4-point Kelvin structures are designed and extensively used to characterize and study performance of micro-bumps with respect to their processing technologies, materials used and electromigration properties [2]-[7]. These test structures are also specially processed with metallization lines connecting top and bottom of the micro-bump structures, which are then routed to test pads for probing. Probecards are usually used to test these micro-bumps in the technology development phase. However, in production phase, particularly for 3DIC micro-bump wafer acceptance tests, standard probecards cannot be adopted for micro-bump characterization tests because dedicated Kelvin or daisy-chain



(a) 2 Micro-Bump Test Structure with 2 True Kelvin Probes

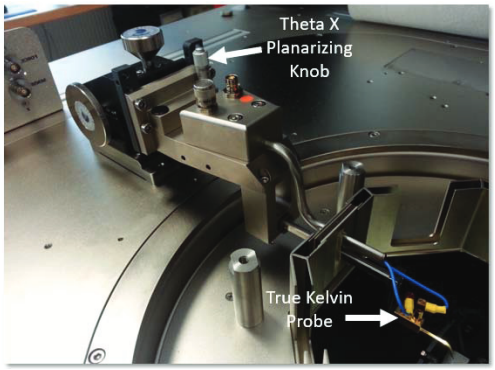
(b) 3 Micro-Bump Test Structure with 3 True Kelvin Probes

Fig. 2. 2-Micro-Bump (a) versus 3-Micro-Bump (b) Test structures with true Kelvin Probes selected from parts of the product.

test structures are usually not included as they will take up additional space.

To determine if the micro-bumping process works well, test engineers, with the help of circuit designers, will identify suitable parts of the circuits on the product that can be utilized as 2- or 3-micro-bump test structures as shown in Figure 2. Instead of test pads, probes will have to land directly on the half-spherical micro-bumps to measure the performance of the micro-bumps. In the example of Figure 2(b), a 3-micro-bump Kelvin test structure is selected from a power line connection where 3 micro-bumps, shorted together to handle higher current are used to accurately measure the resistance of a single micro-bump. Besides testing the micro-bumps, wafer surface leakage current measurements are also mandatory to ensure the process of implementing the copper pillar and micro-bumps do not leave behind any unwanted residual metallization which could result in short circuits.

Making measurements at the wafer surface and on the micro-bumps require probing at different Z contact heights. Henceforth, DC positioners with probe tips are preferred because probecards are not flexible enough to support different contact height requirements. Compared to probecard, DC positioners also offer a lot more flexibilities and can handle any design permutations of micro-bump test structure layouts for different products. However, with DC positioners, test engineers still face challenges in achieving highly accurate and repeatable micro-bump measurements because having standard single DC probes, it is very challenging to have good and stable electrical contact on 25µm or smaller micro-bumps for a fully automated production test requirement. In both cases for the 2- or 3-micro-bump test structures shown in Figure 2, it is extremely tedious and challenging to make good, stable and repeatable electrical contacts with 2 DC probes on the same 25µm micro-bump for force and sense Kelvin measurements because it is equivalent to trying to land the 2 probes on the same test pad which is not planar and smaller than 12.5×12.5µm.

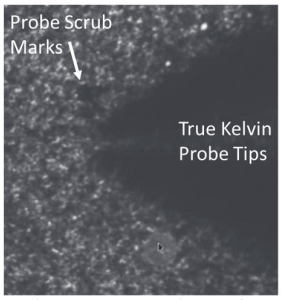


(a) DC positioner with theta X planarizing capability

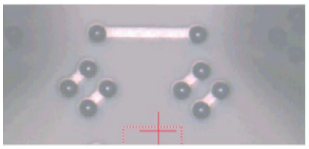
(b) True Kelvin DC probe with pitch 8µm, probe tip radius of 1.5µm

(c) Aluminium contact substrate to planarize the true Kelvin probe

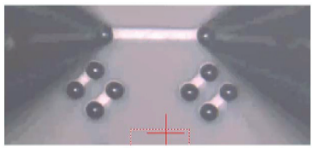
Fig. 3. DC positioner with theta X planarizing Capability (a), true Kelvin DC probe with pitch 8µm, probe tip radius of 1.5µm (b) and aluminium contact substrate to planarize the true Kelvin probe (c).



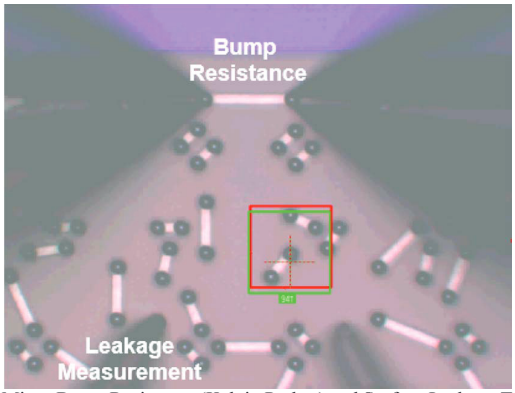
(a) True Kelvin Probes on Contact Substrate for Probe Planarization



(b) Before probing on Micro-bump



(c) True Kelvin Probes on Micro-bumps



(d) Micro-Bump Resistance (Kelvin Probes) and Surface Leakage Tests (Standard DC probes)

Fig. 4. Die photos of true Kelvin probes on planarizing substrate (a), a metal line with 2 Micro-Bump before probing (b), after Kelvin probes are on Micro-Bumps (c) and micro-bump resistance and surface leakage current wafer acceptance tests with 2 standard probes on the wafer surface (d).

In this work, to accurately characterize the resistance of micro-bumps having 25µm diameter, a custom DC positioner with theta-X planarizing capability, custom true Kelvin probes with force and sense probe tips having 1.5µm tip radius and 8µm pitch and aluminium contact substrate for probe planarization are developed as shown in Figure 3. Theta-X planarizing probe positioner and the aluminium contact substrate allow the true Kelvin probe to be planarized before they are used for measurements. This is a crucial step to ensure that both force and sense probe tips are planar to the wafer surface and they can make contact on the micro-bumps at the same time, with the same amount of force during probing.

Figure 4(a) illustrates a die photo showing 1 set of true Kelvin probes on contact substrate for probe planarization. After

the probe tips make contact with the contact substrate, they leave behind probe marks and test engineers rely on these probe marks to make adjustments to the planarity of the Kelvin probe tips using the theta X planarizing knob shown in Figure 3(a). By repeatedly adjusting theta X planarizing knob, re-probing onto the planarizing substrate and examining the probe marks, test engineers can ensure that the true Kelvin probes are flat and planarized before the actual probing and testing on the micro-bumps. After the probes are planarized, 2 sets of Kelvin probes should be probed and electrically shorted on the contact substrate and the resistance of this setup measured to determine electrically if the contact and planarity of all the probe tips are acceptable. The steps described above are particularly critical in achieving stable and repeatable electrical contact when probing on the micro-bumps.

Figure 4(b) shows the micro-bumps prior to probing. Compared to using 2 separate single probe tips, probing micro-bumps with true Kelvin force sense tips allow for "gripping" action on the half-spherical micro-bumps when the probe tips land on the top half of the bump, facilitating good, stable and consistent electrical contacts as depicted in Figure 4(c). It is very important that the true Kelvin probes offer such performance because the series resistance of each micro-bumps is in the order of a few milli-ohms. Figure 4(d) shows die photo of a typical micro-bump wafer acceptance test setup with 2 true Kelvin probes making electrical contact with the 2-micro-bump test structure and another 2 standard probes in contact with the wafer surface to measure the surface leakage current.

III. Results and Discussions

Figure 5 shows the Keysight's semiconductor parametric analyzer and FormFactor's Cascade Microtech 300 (CM300) fully automatic probe system which can support automatic loading and unloading of both 200mm and 300mm wafers. This test system is used to automatically characterize the micro-bump resistance and wafer surface leakage current of 10 wafers having 2-micro-bump test structures and another 10 wafers with 3-micro-bump test structures (refer to Figure 2) in a fully automatic fashion.

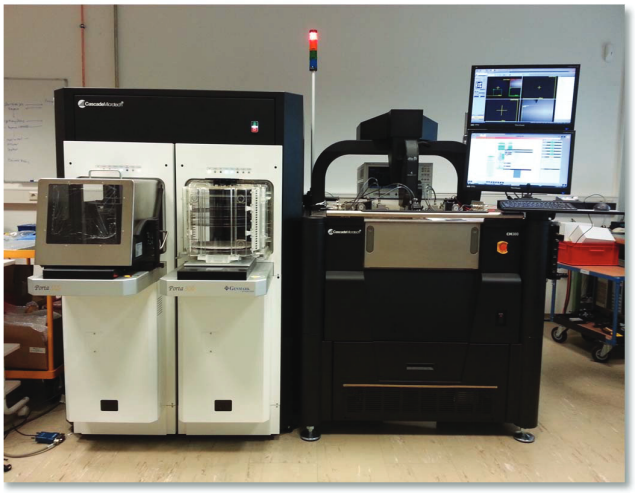
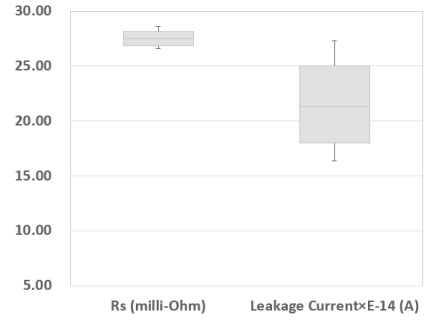
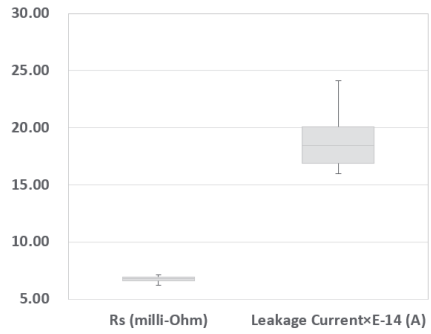


Fig. 5. Cascade Microtech CM300 Fully Automatic Probe System with 200mm and 300mm Wafer Load Ports and Keysight Semiconductor Parametric Analyzer.



(a) 2-Micro-Bump Test Structure



(b) 3-Micro-Bump Test Structure

Fig. 6. Measured Micro-Bump resistance and wafer surface leakage current for 2-Micro-Bump (a) and 3-Micro-Bump Test Structures as shown in Figure 2.

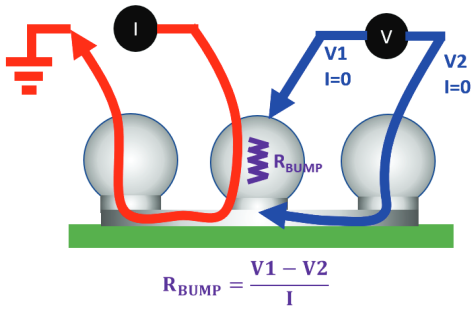


Fig. 7. Calculation of Bump Resistance for 3-Micro-Bump Test structure.

For these micro-bump wafer acceptance tests, usually only the partial dies on the edge of the wafers are selected as test dies. Wafer-edge partial dies are preferred because test engineers are then able to avoid damaging micro-bumps on functional full dies during tests which could render these good dies unusable for the final 3D stacked product. Figure 6 shows the series resistance and wafer surface leakage performance of the 2- and 3-micro-bump on their respective 10 wafers. The wafer surface leakage currents of all the wafers are very low, less than 0.3 pA, showing no residual metallization on the wafer surface after processing the copper pillars and micro-bumps onto all 20 wafers.

Using true Kelvin force sense probes on the micro-bumps, the measured series resistance of the 2-micro-bump test structure varies from 26.6 to 28.6 milli-ohms as shown on the box plot in Figure 6(a). Measured series resistance of the 3-micro-bump test structures varies from 6.2 to 7.1 milli-ohms as shown on the box plot in Figure 6(b). The measured series resistance of the 2-micro-bump test structure is a result of the total resistance of two micro-bumps plus the metallization that connects them. On the other hand, the 3-micro-bump test structure, when characterized in a Kelvin approach outlined in Figure 7, allows test engineers to accurately measure the series resistance of a single micro-bump.

This explains why the 3-micro-bump test structures have much lower series resistance when compared to the 2-micro-bump test structures. Fabless IC companies prefer to use these 3-micro-bump test structures as the test vehicle for wafer acceptance tests because single bump resistance allows for easy performance monitoring of different products which have adopted the same bumping process as well as establishing correlations when different micro-bump size and processing technologies are used. Test engineers, on the other hand, prefer 2-micro-bump test structures because they are much easier to characterize, especially when these engineers only have single DC probes and not true Kelvin probes at their disposal.

The small variations in measured results shown in Figure 6 reveals that the use of true Kelvin probes, which offers a "gripping" action wrapping around the spherical micro-bump to achieve electrical contact, allows for very consistent and repeatable measurements of series resistance for both the 2-micro-bump and 3-micro-bump test structures even when they are tested in a fully automatic fashion with robotic wafer loading and unloading. This would be extremely difficult to achieve if single standard DC probe tips are used, hoping to accurately probe and make electrical contacts with these micro-bumps.

IV. Conclusions

The size of micro-bumps is reducing rapidly as silicon processing technologies continue to improve with strong increasing demands for 3D stacking of dies to push for lower costs, better product performance at higher integration levels. Probecards and Single DC probes are unable to address the challenges and measurement flexibilities needed for micro-bump wafer acceptance tests, especially when direct probing and measurements on these spherical micro-bumps are required.

When DC positioners with theta-X planarizing capability, contact substrate for probe planarization and custom true Kelvin probes are used to probe and measure the series resistance of 25µm micro-bumps, accurate and repeatable measurements can be achieved. This unique micro-bump probing solution together with single DC probes for characterizing wafer surface leakage performance, when used in a fully automatic micro-bump wafer acceptance test setup, have enable highly precise and consistent capturing of test results for multiple test wafers as demonstrated in this paper.

References

[1] Kwangsoo Han, Andrew B. Kahng, JiaJia Li, "Improved performance of 3DIC implementations through inherent awareness of mix-and-match die stacking" Proc. Design, Automation & Test in Europe Conference & Exhibition (DATE), 2016.

[2] Da-Quan Yu, Tai Chong Chai, Meei Ling Thew, Yue Ying Ong, Vempati Srinivasa Rao, Leong Ching Wai, John H. Lau, "Electromigration study of 50 µm pitch micro solder bumps using four-point Kelvin structure", Proc. 59th Electronic Components and Technology Conference, pp 930-935, 2009.

[3] L. Xu, J. K. Han, J. J. Liang, K. N. Tu, and Y. S. Lai, "Electromigration Induced High Fraction of Compound Formation in SnAgCu Flip Chip Joints with Copper Column", Appl. Phys. Lett., Vol. 92, (2008), pp. 262104-1.

[4] Y. W. Chang, T. H. Chiang, and C. Chen, "Effect of Voids Propagation on Bump Resistacne due to Electromigration in Flip-Chip Solder Joints Using Kelvin Structure", Appl. Phys. Lett., Vol. 91, (2007), pp. 132113-1.

[5] Y. W. Chang, H. Y. Peng, R. W. Yang, Chih Chen, T. C. Chang, C. J. Zhan, J. Y. Juang, "Analysis of bump resistance and electrical distribution of ultra-fine-pitch microbumps" Proc. 2010 5th International Microsystems Packaging Assembly and Circuits Technology Conference, pp. 1-4, 2010.

[6] Yu-Min Lin, Chau-Jie Zhan, Jing-Ye Juang, John H. Lau, Tai-Hong Chen, Robert Lo, M. Kao, Tian Tian, King-Ning Tu, "Electromigration in Ni/Sn intermetallic micro bump joint for 3D IC chip stacking", Proc. IEEE 61st Electronic Components and Technology Conference (ECTC), pp. 351-357, 2011.

[7] Hsiao-Yun Chen, Da-Yuan Shih, Cheng-Chang Wei, Chih-Hang Tung, Yi-Li Hsiao, Douglas Cheng-Hua Yu, Yu-Chun Liang, Chih Chen, "Generic rules to achieve bump electromigration immortality for 3D IC integration", Proc. IEEE 63rd Electronic Components and Technology Conference, pp. 49-57, 2013.