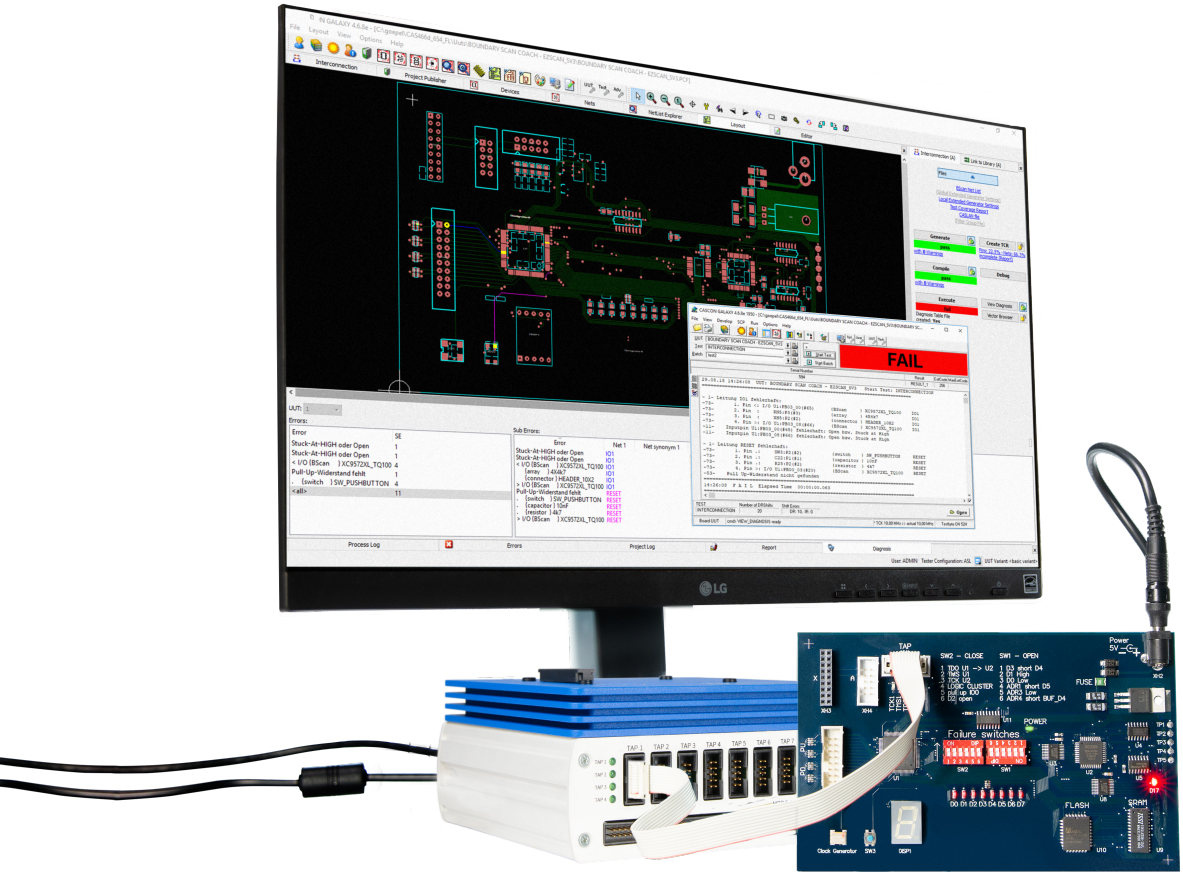
Embedded JTAG Solutions

Application

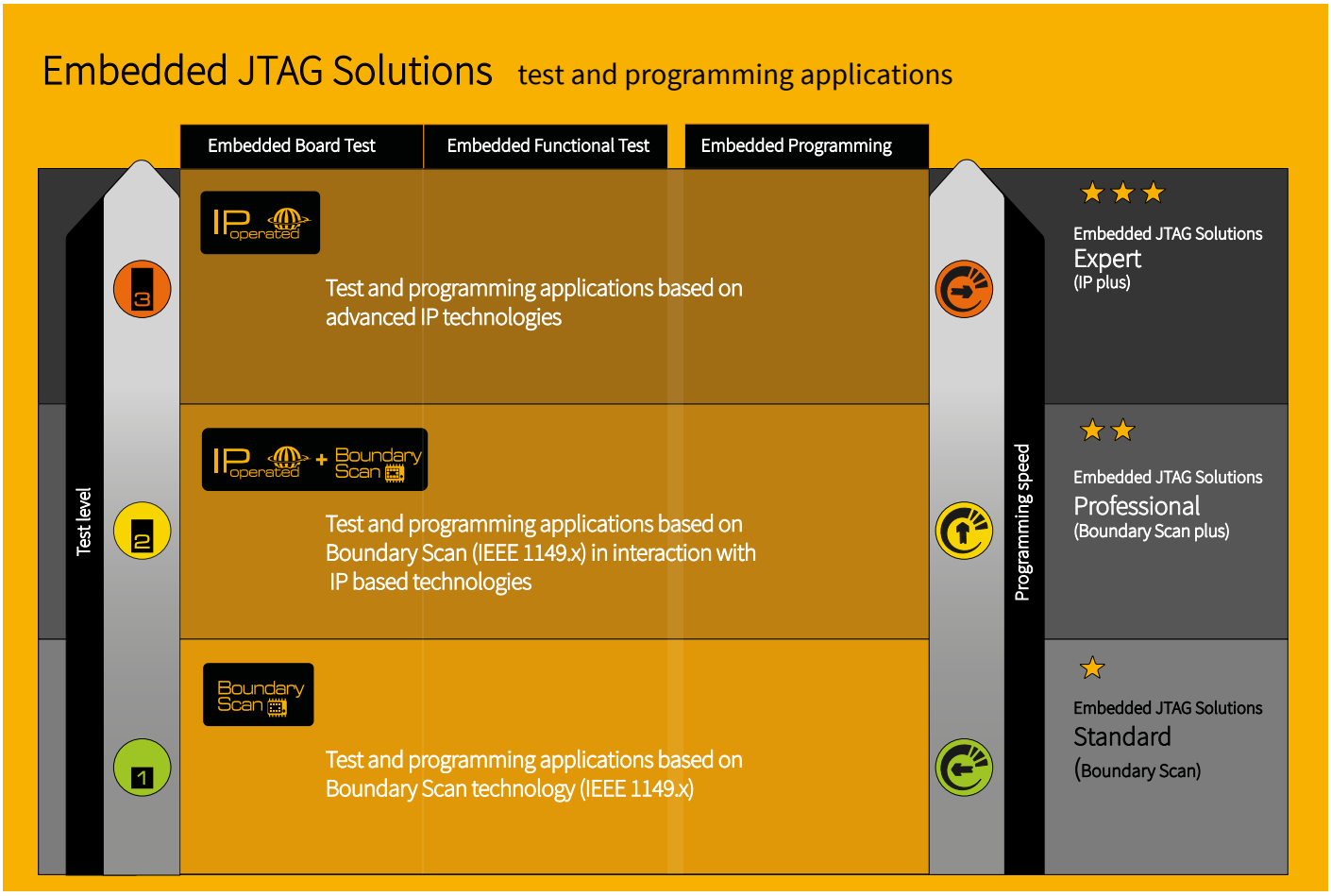


- test development independent of software or firmware development status
- fast error detection on prototypes for better time-to-market
- pin-accurate diagnosis
- combination of test and programming
- parallel processing of several test targets
- combination of structural and functional test
- easy automation
- generation of safe test vectors
- integration of safety and security mechanisms

GOEPEL electronic

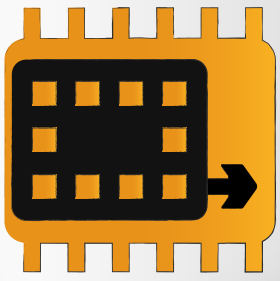
Enjoy Testing

EJS matrix



Embedded JTAG Solutions

In the electronics industry, ICs are becoming ever smaller and the packing density is increasing. As a result, access via pins is decreasing rapidly. For this reason, a test procedure has been developed which can control and measure almost every pin via a serial sliding chain.
Typically 4 signals are required for this. This method became known as JTAG/Boundary Scan and was standardised in 1990. JTAG/Boundary Scan offers unique possibilities for expansion due to its open architecture and the versatility of the JTAG interface. These characteristics make JTAG/Boundary Scan a technological basis for new, non-intrusive access methods and standards for testing, debugging, programming and emulation: the Embedded JTAG Solutions.



Embedded Board Test

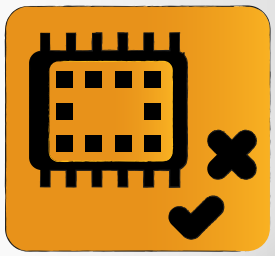
Embedded Board Test

The embedded board test is used to verify connections on a module. All possible boundary scan, microcontroller and FPGA resources are used here to detect short circuits, unsoldered pins or missing pull resistors.

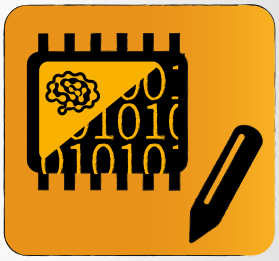
EJS matrix

Embedded JTAG Solutions test and programming applications

IP = Intellectual Property



Embedded Functional Test



Embedded Programming

Embedded Functional Test

Today's test strategies require more than just the simple testing of structural assembly connections. In addition to perfect contacting, functional assembly and component functions must also be tested. This is where the embedded functional test comes into play.

Embedded Programming

In addition to testing, programming also plays programming also plays a major role in the production of assemblies. Increasing data volumes in particular pose a major challenge. The Embedded JTAG Solutions offer an optimal, flexible solution for programming, individually or in parallel.

Application overview

Application	Tool/Licence	CASCON GALAXY						Hardware platform		Performance			
		Pin Access	Base	Standard EJS	Professional	Expert	ISP	SCB II	SFX II	Static	At-Speed	Nominal	Stress
Infrastructure test	ATPG Infrastructure	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	
Connection test	ATPG Interconnection 1149.1 & 1149.6	opt	✓	✓	✓	✓	X	✓	✓	✓	✓		
RAM Connection test	ATPG Memory Access	opt	opt	✓	✓	✓	X	✓	✓	✓			
Logic clustertest	ATPG Clusters (Truth Table)	opt	opt	opt	opt	✓	X	✓	✓	✓			
	ATPG Logic Components												
Logic clustertest	ATPG Clusters (Wave Form)	opt	opt	opt	✓	✓	X	✓	✓	✓			
Boundary Scan with Flying Probe or ICT Test	ATPG Interactive ATE	opt	opt	opt	opt	opt	X	✓	✓	✓			
Component test - model based (e. g. LED, Clock)	ATPG Device Model	opt	opt	✓	✓	✓	X	✓	✓	✓			
Embedded Built in Self Test	Basic Test Generation	✓	✓	✓	✓	✓	X	✓	✓	✓			
FPGA - RAM Connection test*	ATPG Memory Access	opt	opt	✓	✓	✓	X	✓	✓		✓		
FPGA - functional RAM Connection test*	ATPG Memory Access	opt	opt	✓	✓	✓	X	✓	✓			✓	
FPGA - RAM Stress Test*	ATPG Memory Access	opt	opt	✓	✓	✓	X	✓	✓				✓
FPGA Frequency measurement*	Basic Test Generation	✓	✓	✓	✓	✓	X	✓	✓			✓	
FPGA Bit Error Rate Test (BERT)*	Basic Test Generation	✓	✓	✓	✓	✓	X	✓	✓			✓	
FPGA Ethernet Fram Error Rate Test (FERT)*	Basic Test Generation	✓	✓	✓	✓	✓	X	✓	✓			✓	
µP - Connection test*	Basic VarioTAP Test Generation	opt	opt	opt	✓	✓	X	✓	✓			✓	
µP - RAM-Connection test*	AVTG Dynamic Memory Access	opt	opt	opt	✓	✓	X	✓	✓			✓	
µP - RAM Stress Test*	AVTG Dynamic Memory Access	opt	opt	opt	✓	✓	X	✓	✓				✓

Application overview

Application	Tool/Licence	CASCON GALAXY						Hardware platform		Performance			
		Pin Access	Base	Standard EJS	Professional	Expert	ISP	SCB II	SFX II	Static	At-Speed	Nominal	Stress
µP - GPIO/ADC/ DAC-Test*	Basic VarioTAP Test Generation	opt	opt	opt	✓	✓	X	✓	✓			✓	
µP - Interface Test*	Basic VarioTAP Test Generation	opt	opt	opt	✓	✓	X	✓	✓			✓	
µP - Systembus Test*	Basic VarioTAP Test Generation	opt	opt	opt	✓	✓	X	✓	✓			✓	
µP - System Cluster Test*	Basic VarioTAP Test Generation	opt	opt	opt	✓	✓	X	✓	✓			✓	

✓ Support up to maximum speed ✓ Limited performance X not possible opt available as a separate software option

Programming overview

Programming	Tool/Licence	CASCON GALAXY						Hardware platform		Performance			
		Pin Access	Base	Standard EJS	Professional	Expert	ISP	SCB II	SFX II	Static	At-Speed	Nominal	Stress
Flash (SPI/I²C/NAND /NOR/eMMC)	Automated Flash ISP (AFPG)	opt	opt	✓	✓	✓	✓	✓	✓	✓			
PLD/FPGA	PLD Program Generators	opt	opt	✓	✓	✓	✓	✓	✓			✓	
FPGA - Flash (SPI/I²C/NAND/ NOR/eMMC)	Automated Flash ISP (AFPG)	opt	opt	✓	✓	✓	✓	✓	✓		✓		
FPGA - Boot Flash (SPI/I²C)	Automated Flash ISP /AFPG)	opt	opt	✓	✓	✓	✓	✓	✓			✓	
µP - Onchip-Flash*	Automated VarioTAP Flash ISP	opt	opt	✓	✓	✓	✓	✓	✓			✓	
µP - Flash (SPI/I²C/NAND/NOR/ eMMC)*	Automated VarioTAP Flash ISP	opt	opt	✓	✓	✓	✓	✓	✓			✓	
X-BUS (SPI/I²C/NAND/NOR/ eMMC)*	X-BUS Scripting	opt	opt	opt	opt	✓	opt	✓	✓			✓	

✓ Support up to maximum speed ✓ Limited performance X not possible opt available as a separate software option

Visualisation tools & features

Visualisation tools & Features	Tool/Licence	CASCON GALAXY						Hardware platform	
		Pin Access	Base	Standard EJS	Professional	Expert	ISP	SCB II	SFX II
Pin Toggler	ScanAssist Multi Mode Debugger	✓	✓	✓	✓	✓	X	✓	✓
Multi Mode Debugger	ScanAssist Inter-active Pin Toggler	✓	✓	✓	✓	✓	X	✓	✓
Automatic scan chain detection	Visual Project Explorer - VIPX	✓	✓	✓	✓	✓	X	✓	✓
Visualisation in the PDF circuit diagram	Scan Vision III Schematic Reader Scan Vision III Schematic Viewer	opt	opt	opt	opt	opt	X	✓	✓
Visualisation in the board layout	Scan Vision III Schematic Reader Scan Vision III Schematic Viewer	opt	opt	opt	✓	✓	X	✓	✓
VIPX netlist	Visual Project Explorer - VIPX	✓	✓	✓	✓	✓	X	✓	✓

✓ Support up to maximum speed ✓ Limited performance X not possible opt available as a separate software option

Performance

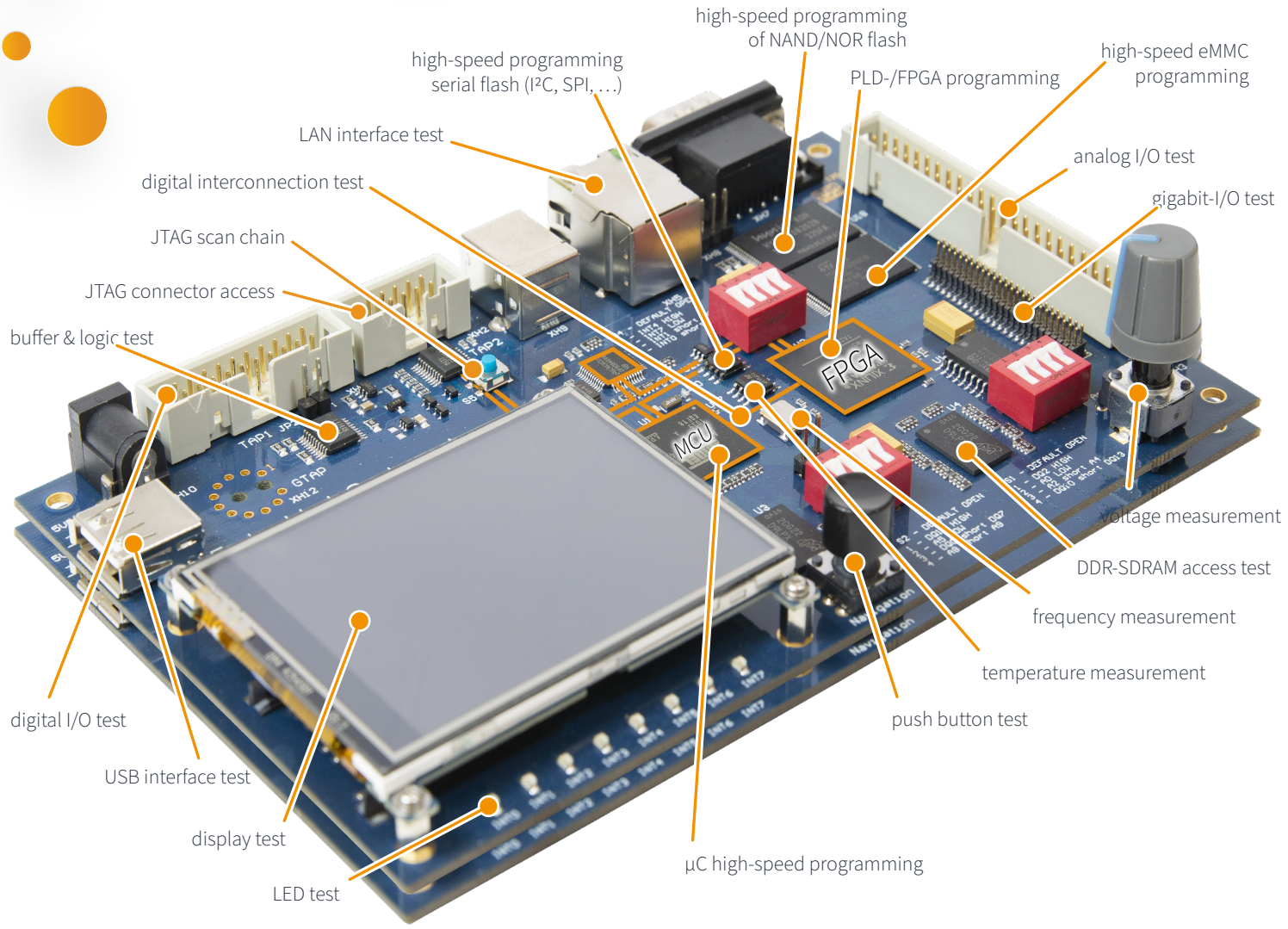
Static	Signal changes take place very far (by orders of magnitude) below the functional speed of the controlling pin
At-Speed	Signal changes take place below the functional speed of the controlling pin
Nominal-Speed	Signal changes take place at the functional speed of the controlling pin
Stress	Signal changes take place at the functional speed and different parameterisation or at a higher speed and/or different parameterisation of the controlling pin

Application

Classification of applications

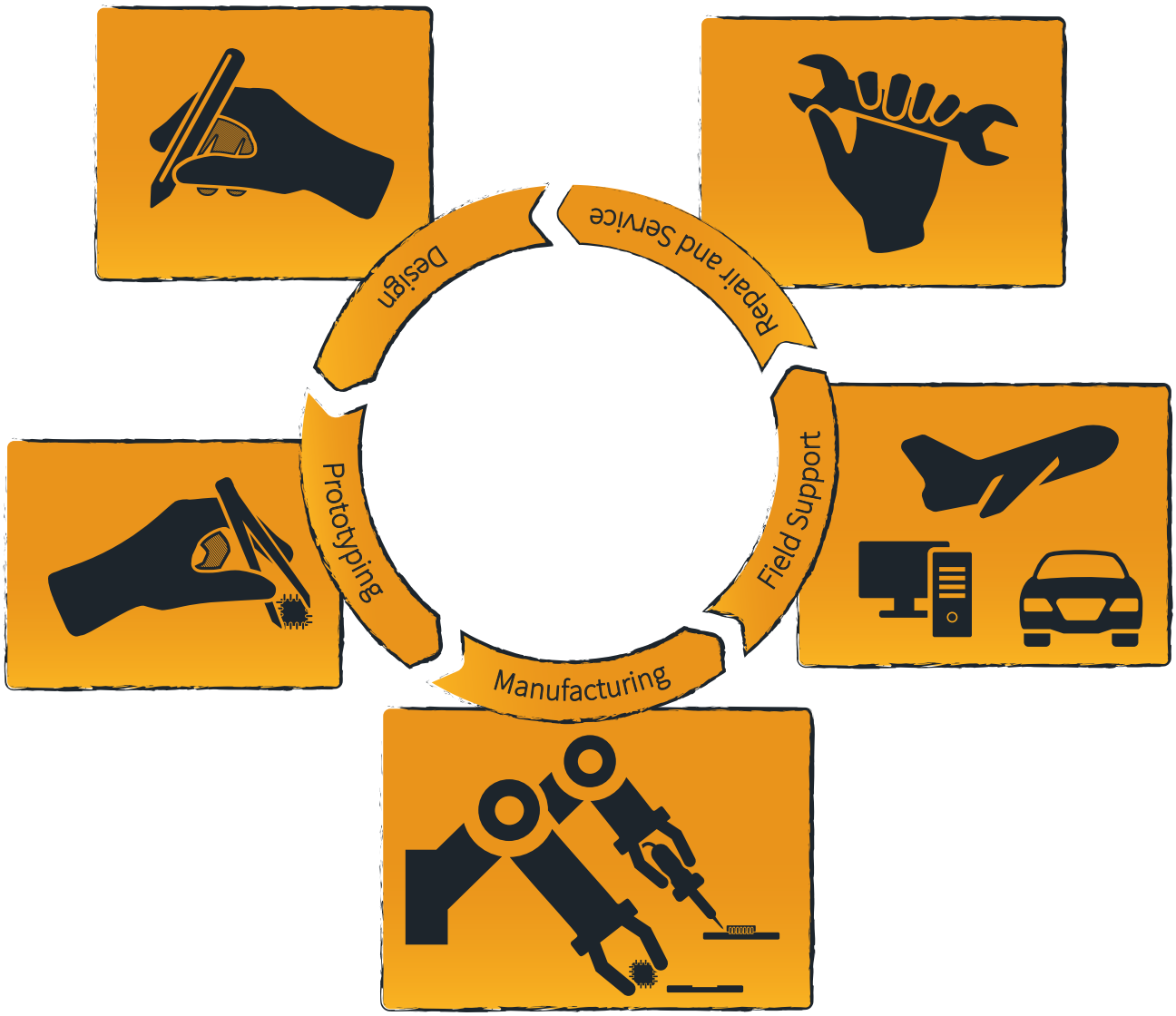
Each step in the program flow has a certain basic goal, such as testing, programming, HW debugging or validation; it is defined by very specific characteristics, such as the instrument used, the execution environment, the execution speed or even interactions with other instruments.

Application type	Key application contents
structural test	structures like pins/nets are tested, but component functionality (other than transparent logic and bus drivers) are not
semi-structural test	test of the same elements as in structural testing, but the test procedure is integrated into a functional framework, e.g. in BERT, data streams are evaluated to assess signal quality
functional test	test of functional elements, e.g. decoders, oscillators, multiplexers, interfaces or others
parametric (analogue) test	test of parameters (e.g. frequency of an oscillator signal, voltage values...) using CION-LX I/O modules and µP-GPIO/ADC/DAC test resources
HW-debugging/validation	interactive test of register structures, pins, connections or logic functions and comparison against specifications, modelling ...
programming	programming of non-volatile memory, such as µP-internal flash, NAND, NOR, eMMC, SPI, I²C, PLD/FPGA or others



Practical application examples

Product life cycle overview



PLC state	typical requirements
design	detailed/accurate DfT analysis to enhance defect coverage and reduce manufacturing cost
prototyping	verification of important signal connections and functional parameters, e.g. correct clocks
manufacturing	highly effective fault recognition with detailed reporting for rapid localization
field support	fast secure firmware updates
repair/service	test, fault localization and updates

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