# CCPMC-SyncClock32-UNIV
# CONDUCTION COOLED

- **IRIG A & B, NASA 36 and 1 PPS inputs**
- **HaveQuick sync option**
- **Propagation delay compensation**
- **Zero latency time reads**
- **Match time output**
- **External event time tags**
- **Three user programmable rates**
- **Conduction cooled**



The CCPMC-SyncClock32-UNIV from Brandywine Communications is an advanced Mezzanine Card (PMC) module. Precision time is provided to the host computer with zero latency. The on-board microprocessor automatically synchronizes the clock to reference signal inputs. The reference signal inputs handled by the PMC in its standard configuration are IRIG's A and B, NASA 36 and 1 PPS. Alternatively, the clock in the PMC can be set using commands from host computer and free run using its on-board oscillator as the time base.

When synchronizing to time codes or 1 PPS the microprocessor constantly measures the time error between the on-board clock and the reference input code and adjusts the error measurement for propagation delay. When the disciplined TCXO option is selected the residual error is used in an adaptive gain loop to adjust the frequency of the 10 MHz oscillator for minimum error. Before being used as the time reference, the input code reference is checked (to code carrier resolution) for consistency with itself. If the incoming code is missing or corrupted by noise the on-board clock is updated by the 10 MHz oscillator. When the input code is again useable the correction loop is smoothly closed.

58 bits of BCD time are available to the host computer using two zero latency time reads. The time message contains units of microseconds through units of years. A status word is available using an additional read.

The time-of-occurrence of external events may be captured (time-tagged) by using the Event Time input. When the event input is sensed the current time is saved in a buffer for later interrogation by the host. The resolution of the time tag is 100 nanoseconds.

The Match Time feature may be used to automatically initiate or terminate an external process. The resolution of the Match Time comparison is one microsecond. The Match Time output is asserted when the time of the internal clock matches that of the user input start time. The Match Time output may be terminated by a user command or when the previously set stop time is encountered.

Three user programmable pulse rates are provided. Two pulse rates, Clock Low and Clock High, are available on the multi-pin connector. The third pulse rate provides heartbeat timing to the host computer and is also available on the multi-pin connector. The divider for each of the three pulse rate generators is programmable by the host computer over the range 2–65,535. The inputs to the rate generators are 3 MHz or 100 Hz for the heartbeat, 100 PPS for Clock Low and 3 MHz for Clock High.

# CCPMC-SyncClock32-UNIV Conduction Cooled Specifications

## General Input Specifications

| | |
|---|---|
| Input Codes | IRIG's A & B, NASA 36 |
| Input amplitude | .25 to 10 Vpp |
| Input impedance | >10k Ohms |
| Ratio | 2:1 to 4:1 |
| Frequency error | 100 PPM maximum |
| Code sync accuracy | One microsecond |
| 1 PPS Input | RS-422 or TTL, positive edge |
| 1 PPS sync accuracy | 300 nanoseconds |
| External Event | |
| Resolution | 100 nanoseconds–units year |
| Min. event spacing | None |

## General Output Specifications

| | |
|---|---|
| IRIG B DC Shift | TTL |
| Match Pulse | TTL level at Start–Stop time |
| Resolution | Microseconds–eight millisecond |
| Clock Low | TTL, negative going |
| Clock Divisor | 2–65,535 |
| Clock Input | 100 PPS |
| Default output | 1 PPS |
| Clock High | TTL, negative going |
| Clock Divisor | 2–65,535 |
| Clock Input | 3 MPPS |
| Default output | 76.923 kPPS |
| Heartbeat Rate | Interrupt, flag, TTL, negative going |
| Clock Divisor | 2–65,535 |
| Clock Input | 100 PPS or 3 MPPS |
| Default output | 1 kPPS |
| BCD Time | Microseconds–unit year on demand, zero latency 58 bits in two 32 bit words |
| Status word | 8 bits |
| Status LED | Flashes coded patterns |
| Interrupts | External Event, Heartbeat, Match Time |
| Flags | Dual Port RAM data ready, FIFO data ready, In sync, Heartbeat, Match Time, External Event |
| Connectors | AI I/O on P4 connector |

***MTBF*** — 141,000 hours per Mil-217-F, Notice 2, 25° C, ground benign

## Mechanical & Environmental

| | |
|---|---|
| Size | 74mm X 149mm single CMC |
| Type | Single-slot 32 bit 5V PCI |
| Power | |
| +5V | ±5%, .15A max |
| +3.3V | ±5%, .25A max |
| -12V | ±5%, .05A max |
| +12V | ±5%, .06A max |
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -40°C to +85°C |
| Humidity | To 95% without condensation |
| Cooling bar locations | Primary and Secondary |

## Options

| | |
|---|---|
| On-board GPS | Trimble Copernicus (GPS antenna connection through front SMB) |
| Input Code Isolation | Transformer coupling |
| Input Codes | IRIG G, XR3, 2137, IRIG E, 109-60 |
| Output Codes | IRIG A, NASA 36 |
| Eight External Event Inputs | TTL, positive or negative edge |
| Have Quick Input | Per ICD–GPS–060 |
| Binary Time Words | Replaces BCD |
| Oscillator Upgrade | Disciplined TCXO, .28 PPM |
| FIFO for external events | Includes interrupt |
| Conformal Coating | Optional Conformal Coat |

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*Other* products

**Video Character Inserters**
**Time-Message Displays**
**VME, PMC, PC/104, PCI, CPCI (3U and 6U), ISA Computer Clock Synchronization Boards**
**Network Time Servers**
**Frequency Generation and Distribution Instruments**
**Dual & Triple Redundant Systems**

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