FOCUS MICROWAVES

Compact Modeling

The intutitive advanced compact model

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Introduction | Compact Model

The Focus Compact Model (FCM) is a software package that is specifically designed to work with Focus' AURIGA high-end pulse system. This package is used to create Compact Models for transistors based on their Pulsed-IV and wide-band pulsed S-parameter data.

The software generates a network of lumped circuit elements that accurately represent the fundamental linear and non-linear behavior of the device across a wide range of bias conditions, frequency and power. The output of the modeling process is a netlist that is compatible with commonly used CAD tools in RF/microwave Design, such as Cadence AWR Microwave Office™ Software and Keysight PathWave Advanced Design System™.

Key features of the FCM:
Linear and Non-Linear Compact Transistor Model Extraction of III-V materials (GaN HEMT or similar technologies).
High frequency FET model parameters from a combination of pulsed DC and S-parameter measurements.
Gate-lag and drain-lag trapping.
Basic thermal model extraction.

Linear Model:
8 Extrinsic parameters (RG, RD, RS, LG, LD, LS, CPG, CPD)
8 Bias dependent Intrinsic parameters (RGD, Ri, CGS, CGD, CDS, GM, RDS, Tau)

Non-Linear Model:
NL Capacitances CGS & CGD
NL Current Sources IDS
NL Diodes DGS & DGD
Export Capability to ADS™ and MWO™.

Simulation

Measurements

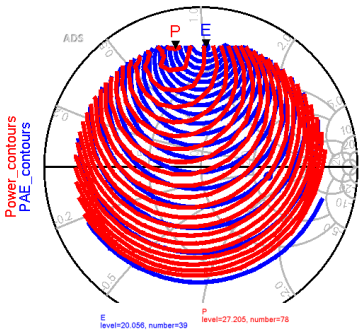
Experimental conditions:

Vgs = -3.3 V Vds = 40 V Ids = 30mA Pavail_in=10dBm Freq = 2GHz

Source Impedances (Polar) F0: 0.80, 150.02° F1: 0.00, -171.71° F2: 0.66, -98.33°

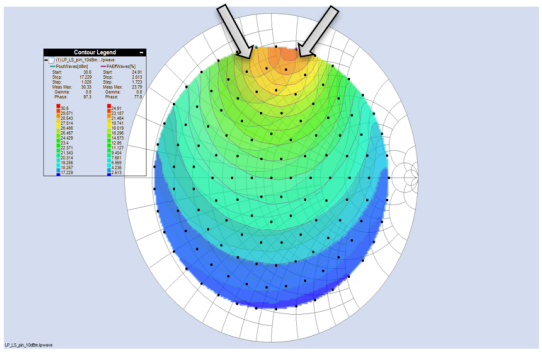
Pdel_dBm Max	27.232
Max power Rho	0.763/101.702

PAE Max	20.076
Max PAE Rho	0.747/88.305



Pout Max	27.18 dBm
Max power Rho	0.8/97.3

PAE Max	20.091
Max PAE Rho	0.8/77.8



HEMT Equivalent Circuit

The objective of creating an electrical representation or equivalent circuit using lumped circuit elements for HEMT or any other transistor is to facilitate its static and RF behavior simulation in CAD tools. This approach is particularly advantageous as it is often directly linked to physical entities present in the device structure, as depicted in the figure.

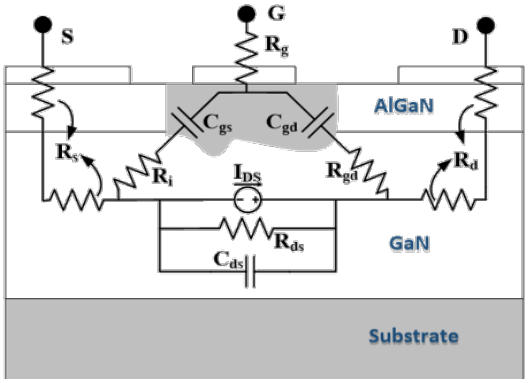
The electrical representation consists of two parts:

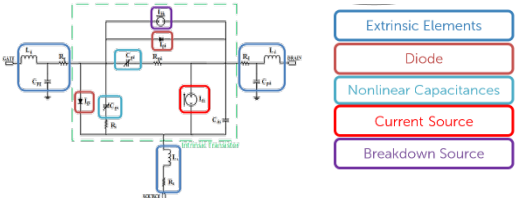
i) The intrinsic part, which comprises the area under the gate where modulation occurs. It is represented by a set of eight intrinsic elements, including RGD, Ri, CGS, CGD, CDS, GM, Tau, and RDS.

ii) The extrinsic part, which is represented by a set of eight extrinsic elements such as RG, RD, RS, LG, LD, LS, CPG, and CPD. These elements need to be extracted for implementing a small signal model.

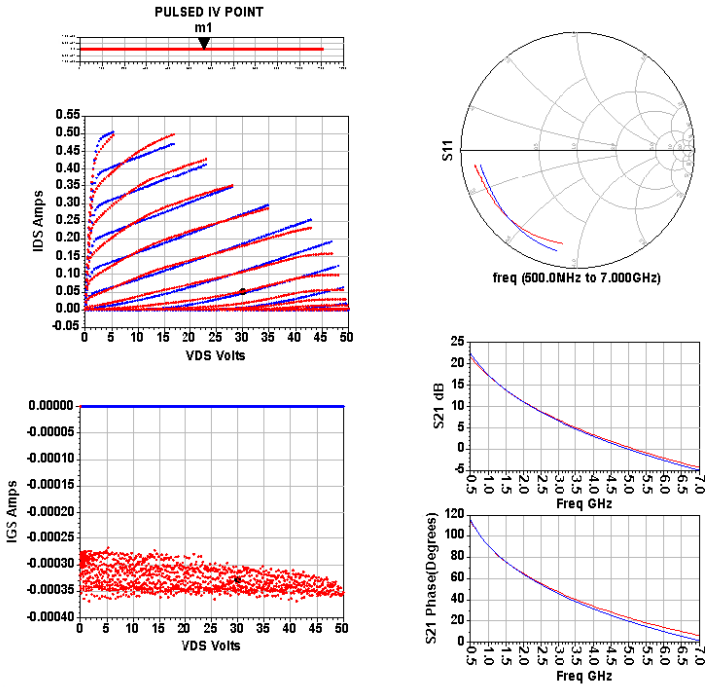
The extraction process for these elements is discussed in the following sections.

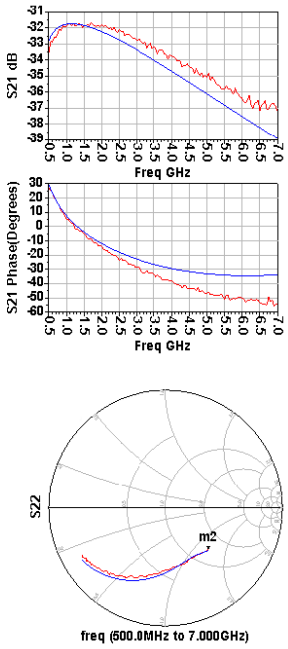
AlGaN/GaN HEMT transistor





Keysight ADS Data Display





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Extraction & Example

The extraction of the linear model is a critical step as it serves as the foundation for developing the non-linear model. This process involves the following steps:

i) Initially, extrinsic values are used to de-embed the S-parameters at the transistor's intrinsic refer ence plane.

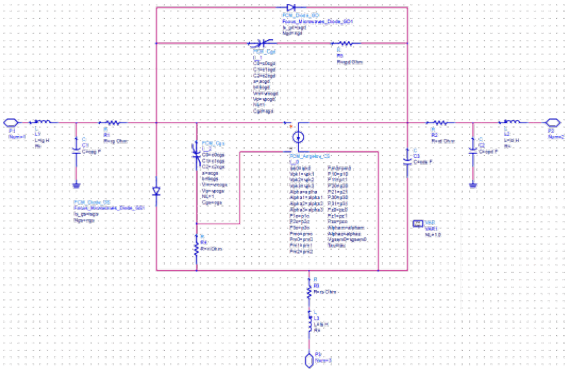
ii) The intrinsic elements are explicitly calculat ed for each frequency using the intrinsic S-parameter measurements. These parameters must be independent of frequency, which is verified during the optimization process.

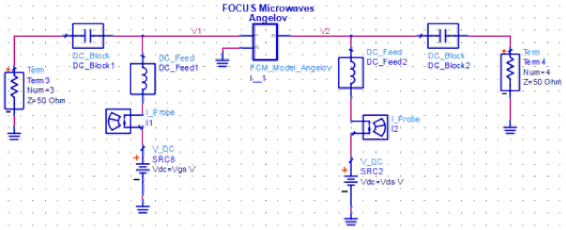
iii) If the intrinsic elements are frequency depen- dent, a new set of extrinsic elements is provided.

iv) An optimization algorithm is implemented in a loop to generate iterative steps for the extrinsic parameters that produce an accurate set of extrinsic elements. These elements are bias-independent.

EDA example

The Focus Compact Model portfolio is fully supported in all major CAD tools including Cadence AWR Microwave Office™ Software and Keysight PathWave Advanced Design™ System.





Optimization Process