

Technologies for Very High Bandwidth Real-time Oscilloscopes

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Invited Paper

Abstract—Technologies and design considerations are presented for the design of very high bandwidth oscilloscopes. These include chip, DSP and microwave technologies employed in some of the fastest waveform digitizers in the world.

Index Terms—Analog-digital conversion, Signal processing, Signal sampling, Signal restoration, Microwave frequency conversion, Oscilloscopes, Oscillography, Indium phosphide.

I. INTRODUCTION

THIS PAPER will present various topics regarding IC design and system architecture that are considerations for the design and production of very high-speed real-time oscilloscopes. Briefly, a real-time oscilloscope is, at the heart, a waveform digitizing instrument that acquires waveforms in a single trigger event. This means that, once armed, it must digitize every waveform point at a given sample-rate, one point after another. It cannot benefit from assumptions of repetitiveness of a signal. For the purpose of this paper, we consider very high-speed real-time oscilloscopes as those occupying bandwidths in the range of tens of Gigahertz to around one hundred Gigahertz with commensurate sample-rates that satisfy the Nyquist criteria of acquiring the entire band from DC to the bandwidth with enough sample rate for there to be no frequency aliasing of the signal. Generally, this means sample rates of around three times the bandwidth. Finally, the record length required for such oscilloscopes depends on the application, but a general goal is to acquire tens of milliseconds of data per acquisition.

II. THE MOORE'S LAW OF SCOPE BANDWIDTH

In Figure 1 we see the progression of oscilloscope bandwidth over time for real-time scopes. This plot shows only scope introductions that represent the highest bandwidth scope from each the three high-end vendors. Here we see a steady log-linear progression that is shown as the line marked *LeCroy Trend* which is the trend considering only scopes manufactured by Teledyne LeCroy - but which is fairly representative of the entire data set. The trend indicates an average yearly increase in bandwidth of approximately 28 percent which amounts

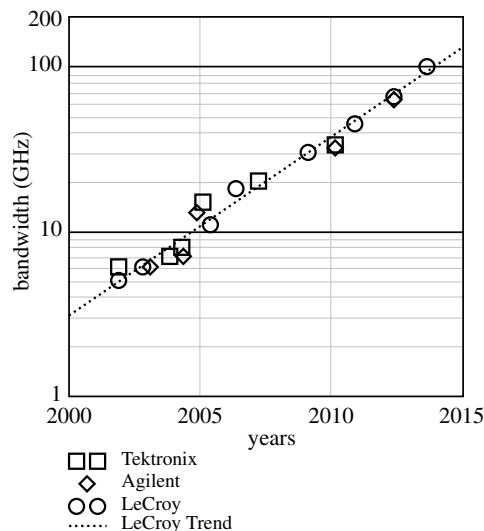


Figure 1. Oscilloscope Bandwidth Versus Time During the Last Decade

to a doubling of bandwidth every 2.8 years. While the plot covers only the first decade of this century, this trend has been fairly constant for the last thirty five years. This leads to the conclusion:

The oscilloscope bandwidth progression is simply another expression of Moore's Law.

While often misstated, Moore's law [1] states that transistor density doubles every 18 months. It says nothing about speed and the implication is that this doubling of transistor density is economical. However, so far, this doubling has been economical and has mostly come with higher speed. Transistor speed is roughly inversely proportional to minimum line thickness and using this loose rule-of-thumb we would predict transistor speed to double every 36 months, or three years. Cause and effect, however, is difficult to interpret. Transistor speeds have certainly benefited over time, but lately, there is little connection between the number of transistors packed into a CMOS microprocessor chip and the speed of bipolar transistor technology which would be used for a scope front-end. Our theory is that the bandwidth progression is *driven* by testing needs as opposed to being enabled by chip technology.

As a final note on this topic, it would be wrong to connect the real concept behind Moore's Law to oscilloscopes because of the economics involved. The cost of an oscilloscope has increased linearly with bandwidth while the cost of computers

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(and related products) have decreased while growing in performance. This is partly because the volume for oscilloscopes is comparatively very small.

III. THE MAIN TECHNOLOGY VECTORS FOR DIGITAL OSCILLOSCOPES

Oscilloscope performance is pushed to higher speeds along three key technology vectors. These are:

- 1) Chip Technology - chips are custom designed in high-speed processes for increasing speed.
- 2) DSP and Corrections Technology - as speeds are pushed, signal fidelity degrades near the upper limits. Signal fidelity is restored through the use of digital signal processing (DSP) and other correction algorithms. Sometimes, this allows the chips to be pushed higher in speed.
- 3) DBI Technology - digital bandwidth interleaving (DBI) is a technology that allows for the doubling and tripling of the speeds limited by chip technology. This is achieved through the combination of channel resources.

Oscilloscope synchronization technology is also utilized to connect multiple acquisition systems to counteract loss of channels through combination of resources.

IV. CHIP TECHNOLOGY

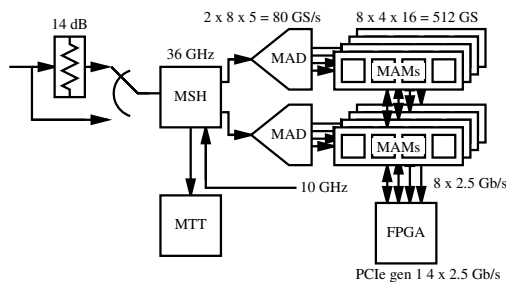


Figure 2. High End Scope Channel Block Diagram

The main technology responsible for oscilloscope performance is chip technology. The underlying performance of a the oscilloscope is determined in the front-end, analog-to-digital converter (ADC) and memory. The front-end is usually a dual-purpose variable gain amplifier and track & hold. Unlike most systems that the reader might be familiar with whereby an analog buffer feeds the ADC containing the track & hold and digitizing elements, in oscilloscopes, because of the speed, the track & hold is generally placed with the amplifier. This is to reduce downstream bandwidth, signal fidelity, and importantly, signal path matching requirements. This is because the digitizer itself might consist of multiple ADC chips and each ADC chip internally consists of multiple ADCs that are time-interleaved. Providing multiple held signals in the amplifier section reduces the bandwidth requirements at the input of the ADC to approximately twice the sample rate of the track & hold which is easier to generate and transmit and is easier to match to each other. The ADC itself has another track & hold whose purpose is to hold this lower speed signal for conversion.

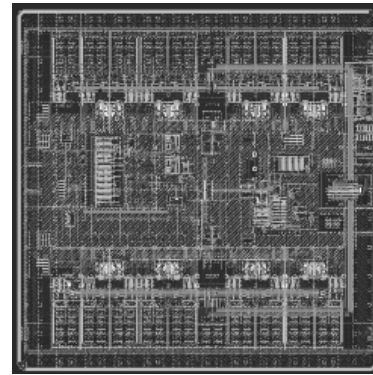


Figure 3. Teledyne LeCroy MSH722B

A high-end LeCroy scope architecture is shown in Figure 2. This is the design of a 36 GHz, 80 GS/s scope channel. It shows an input section which is basically a switched attenuator which provides for 14 dB of attenuation. This feeds an MSH¹ which serves the dual purpose of providing 18 dB of continuous gain in multiple combinations of fixed and variable gain amplifiers and providing sixteen 5 GS/s tracked and held outputs. The MSH is implemented in IBM's 8HP Silicon Germanium (SiGe) process. Each of these outputs has a sample phase that provides for interleaving of the final result. Some interesting features of the MSH is that it consists of sets of gain stages and driver stages that successively fan out the analog signal. The first driver stage drives five outputs, one to the trigger system and four to four drivers which each drive four track & holds. The chip is designed to take its input directly from the center of the chip and to provide its tracked and held outputs on the periphery. The package for the MSH has a built in coaxial connector so that coaxial cables from the outside of the scope are connected directly to the chip package, maintaining a high bandwidth coaxial environment for as long as possible.

Eight of the tracked and held MSH outputs go to one MAD and eight go to another. The MSH also supplies independent sample clocks to each MAD input. Each MAD provides for 40 GS/s sample rate and contains eight virtually independent 5 GS/s internal ADCs. The MAD is implemented in IBM's 7HP SiGe process. Finally, each 5 GS/s data stream is stored in MAMs which are custom designed memories. Each MAM chip takes data at 10 GS/s and can store up to 16 million samples. Note that the MAD provides a data muxing arrangement internally so that even at lower sample rate configurations that might employ less ADCs, these lower number of ADCs can still access the full memory provided by the MAMs.

The readout system consists of an FPGA exposing, on one end, four lanes of PCI Express gen 1 for up to 10 Gb/s (8 Gb/s payload) and on the other end, eight 2.5 Gb/s links that go directly to the MAMs and acquisition system controller in a daisy-chained arrangement. The readout system can sustain approximately 400 MS/s readout rates.

¹There is some special LeCroy nomenclature employed here. All LeCroy chips are referred to as three letters beginning with an 'M' which stands for monolithic. The complete three letter acronym tries to be descriptive. Therefore, an MSH is a monolithic sample/hold, an MAD is a monolithic ADC, and an MAM is a monolithic acquisition memory.

Finally, in Figure 2 we also see one other custom chip, the MTT. This is a combination trigger and timebase chip. It is implemented in IBM 5HP SiGe process and enables smart triggers and is the main acquisition controller.

A. Indium Phosphide Front-end Amplifier

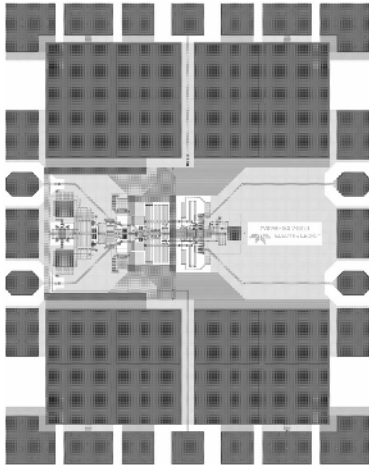


Figure 4. DC-65 GHz Variable Gain Amplifier

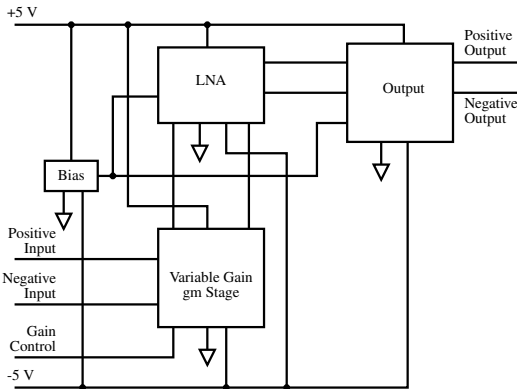


Figure 5. InP Amplifier Block Diagram

After LeCroy joined Teledyne in 2012, Teledyne LeCroy began designing into Teledyne Scientific’s Indium Phosphide (InP) technology [2]. This allows for an increase in front-end performance beyond the current 36 GHz. A goal would be to develop a multi-staged track & hold topology where the InP chip sets the bandwidth.

Most are familiar with III-V processes such as Gallium Arsenide in RF IC design. Despite their high frequency capabilities, the bandwidth of chips developed in these processes tend to be narrow band. In oscilloscope designs, the requirements are for very broad band performance including DC, which is also surprisingly problematic. Another characteristic important for oscilloscope front-ends is thermal tails caused by self-heating of the bipolar devices. Thermal tails cause the step response to slowly reach the final state over a very long (like 1 μ s) time period.

In order to gain familiarity with Teledyne Scientific’s process, an evaluation front-end amplifier was developed. The chip was fabricated using Teledyne Scientific’s 500 nm InP HBT process. The process offers devices with 350 GHz cut-off frequencies, a BV_{cb0} of 5 V, low-loss BCB inter-layer dielectric and four levels of metal interconnect.

The design requirements for an evaluation amplifier were, bandwidth in excess of 65 GHz, signal-to-noise ratio (SNR) of greater than 40 dB, thermal tails less than 1 %, total harmonic distortion (THD) better than -40 dB, and a continuous variable gain range of 10 dB. An amplifier like this would be cascaded with another such amplifier followed by a track & hold in an actual oscilloscope front-end.

A block diagram for the proposed amplifier is shown in Figure 5. Here we have three main sections: a variable gain gm stage, a low noise amplifier (LNA) stage and an output stage. Each stage presents certain challenges which will now be discussed.

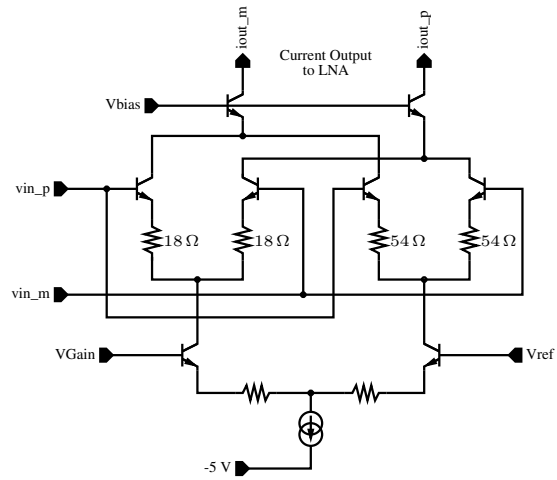


Figure 6. Variable Gain gm Stage (Simplified)

1) *Variable Gain gm Stage:* The variable gain gm stage is shown schematically in Figure 6. The function of this stage is to convert a single ended input voltage to a differential output current. The amplitude of this current is dependent on the gain setting of the stage. In addition, this stage provides the variable gain function. An ideal solution to provide this function would be to use FETs, but these are not available at present, so the solution is entirely bipolar. Our solution to achieve low noise, high bandwidth good linearity and low thermal tails is to connect two long tail pairs in parallel each with a different emitter degenerating resistor and each with a variable tail current. The variable tail current satisfies the continuously variable gain requirement. The tail current is set by the gain control voltage which has a range from -3.5 to -1.5 V which provides continuous variable gain from between 0.98 and 3.35. In order to provide the 40 dB signal to noise ratio large devices were required, which tended to lower the stages bandwidth. By carefully sizing the devices a good compromise for both SNR and bandwidth was achieved.

2) *LNA Stage:* The LNA stage is shown schematically in Figure 7. In order to keep rbb noise to a minimum this stage

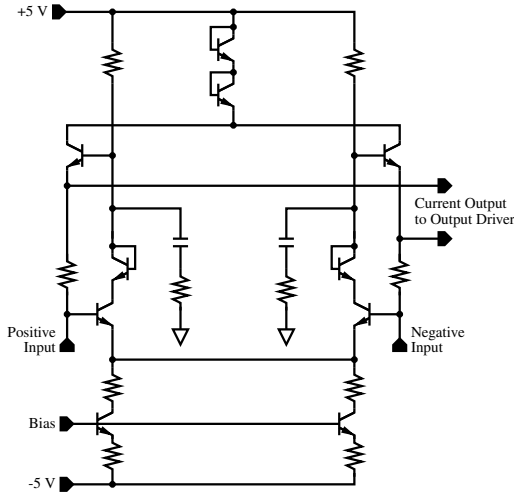


Figure 7. LNA Schematic (Simplified)

requires relatively large devices. By using large devices, the thermally generated rbb noise is kept low, but due to the large capacitance the bandwidth suffered. In order to satisfy both noise and bandwidth, a feedback scheme was used. The large output impedance of the gm stage drives into the low input impedance of this stage’s shunt feedback amplifier. The stability of the amplifier is controlled by an RC network and adjusted for a phase margin of about 55 degrees. This allowed for decent bandwidth but with a slight bit of peaking (about 1.5 dB in simulation before parasitic extraction).

3) *Output Stage:* The low output impedance of the LNA drives into the high input impedance input of the output stage. This stage provides two emitter followers in series to provide the necessary current required to drive the 50 ohm loads to 500 mVpp differential and not present a load to the preceding stage. Two series connected emitter followers could lead to instability. Due to wiring inductance in the base this stage had at least 30 dB of peaking after parasitic extraction. A series resistor added to the base reduced the peaking to around 5 dB.

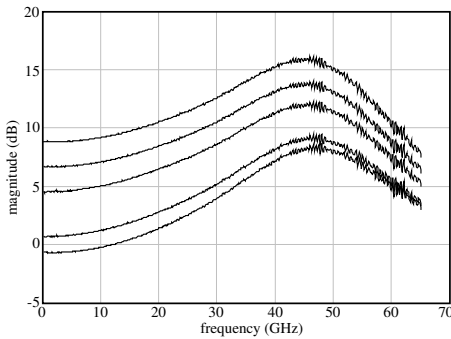


Figure 8. InP Amplifier Frequency Response

4) *Conclusion:* The test chip was fabricated on a multi-project wafer and the die is shown in Figure 4. Parasitic extraction was performed using HFSS® from ANSYS for all wiring and all parasitic models were s-parameters. The extracted simulations utilized very large, multi-port s-parameter blocks with the transistor models reinserted. We found that the use

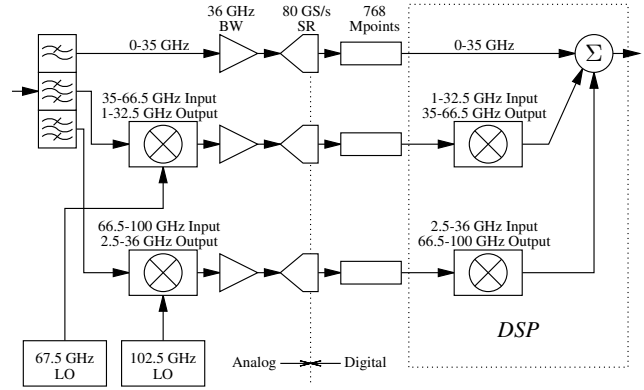


Figure 9. DBI System Block Diagram

of s-parameters does not work well for transient simulations and we are working on a better design/simulation flow.

Comparing the measured results with the simulated extracted results showed a good match. The frequency response is shown with various gain control settings in Figure 8 where we see the expected 5 dB of peaking and in excess of 65 GHz bandwidth.

The chip achieves all of the design goals, but does exhibit about 1.5 dB of compression which will be improved in future versions. Our evaluation shows viability for future oscilloscope designs.

V. DIGITAL BANDWIDTH INTERLEAVING (DBI)

Digital Bandwidth Interleaving, or DBI [3][4] is a Teledyne LeCroy patented technique in which multiple channel resources are combined to an oscilloscope channel that is virtually a combination of the bandwidths of the combined channels. This technique is analogous to the well-known technique of time-interleaving, which combines channel resources to obtain higher channel sample rates. DBI is the only technique that increases both bandwidth and sample rate. This technique has been employed in the design of several generations of high-end oscilloscopes [5][6].

A DBI architecture that utilizes this traditional hardware is shown in Figure 9. In this design, three 36 GHz, 80 GS/s scope channels are utilized. The scope channels are combined with a microwave front-end and a DSP back-end. The combination of channel resources is common in oscilloscope designs and is often selectable by the user.

The microwave front-end shown stylistically in Figure 9 consists of a multiplexer [7][8] that separates the incoming signal into multiple frequency bands feeding multiple down-converters to frequency translate the separate bands down to a frequency range suitable for acquisition by digitizing channels. Note that for the lowest frequency band, no down-converter is employed and the signal is fed directly to the oscilloscope front-end. For the high-frequency bands, the down-converter modules have digitally controllable gain adjust and the usable band does not extend to DC.

Each down-converter consists of variable attenuation and gain elements, a mixer, a local oscillator (LO), image reject filters and fixed gain amplifiers. There are also mechanisms

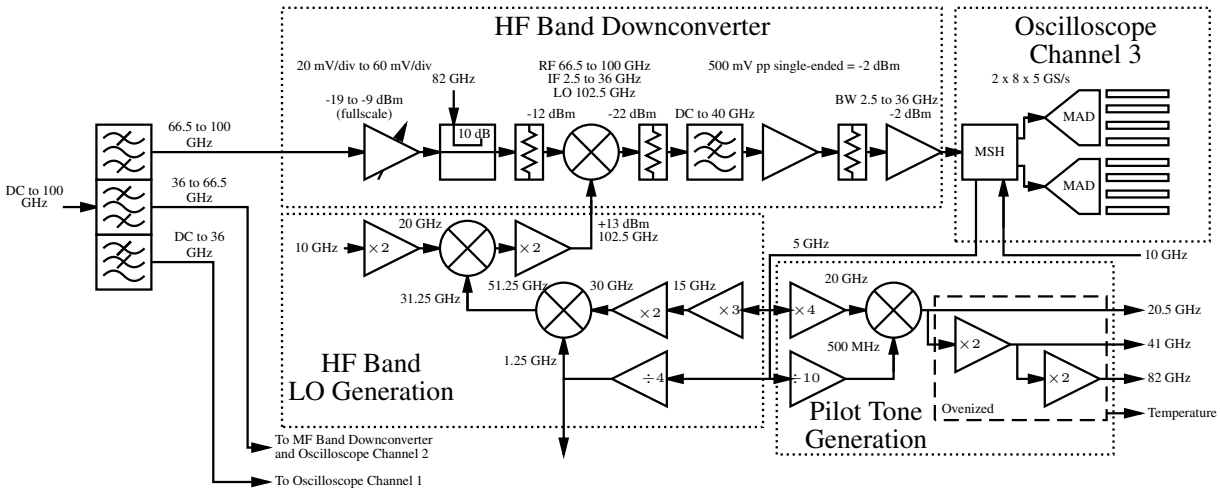


Figure 10. HF Band Down-converter Block Diagram

for locking the reference clock of the LO to the oscilloscope timebase and sample clock generation along with means for inserting similarly locked calibration tones into the mixer [9] radio frequency (RF) inputs in each band for LO phase calibration. These methods are used for subsequent digital LO regeneration.

Each down-converter is driven by a LO that is set higher than the edge of the frequency band. In this way, the input to the down-converter is translated down and flipped over in frequency (i.e. high-side down-conversion is employed).

In this discussion, the following nomenclature is used to refer to the bands:

- LF - low frequency band - DC to 35 GHz
- MF - medium frequency band - 35 to 66.5 GHz
- HF - high frequency band - 66.5 to 100 GHz

On the DSP side, processing is performed to regenerate the input signal from the three 80 GS/s acquisitions. The recombination involves upsampling from 80 to 240 GS/s, digitally synthesizing a phase-locked rendition of the LO, up-converting the signal back to its original frequency band, rejecting unwanted images, and combining the results. The final result is an 100 GHz, 240 GS/s waveform acquisition [10].

A. Downconverter

A detail of the HF downconverter is shown in Figure 10 and is illustrative of all of the downconverters (with appropriate changes of frequency).

In oscilloscope design, one tends to think of signal strength in terms of a full-scale signal at a given volt/division setting. There are eight divisions vertically on an oscilloscope screen². This oscilloscope handles ranges from 10 mV/div to 80 mV/div, thus the scope accepts full-scale signals from approximately -18 to 0 dBm. Thus, after the high frequency band has been split off by the multiplexer, the first task of

the downconverter is to provide variable attenuation and gain such that the signal provided to the high linearity mixer is at a constant maximum level of -10 dBm, set 24 dB down from the LO for maximum mixer spur levels of -41 dBc.

There are additional filters placed before and after the mixer. The initial filter is designed so that no signal in the IF band of approximately 2.5-36 GHz is present at the RF port, otherwise the poor (approximately 15 dB) port-port isolation of the mixer causes spurs in the IF. The final filter is designed to reject mainly the LO that leaks to the IF port at about 0 dBm – this would saturate any downstream amplifier.

The fixed gain IF amplifier at the final stage sets the final output power to -4 dBm, which represents almost the full-scale range of the ADC (reserving 3 dB for digital compensation).

The gain/attenuation of the downconverter is finely balanced to achieve a noise figure of 8 to 18 dB depending on the gain range with a worst case SNR of approximately 34 dB. Regarding linearity, it achieves IM3 of -50 dBm and OIP3 in excess of 19 dBm.

B. Local Oscillator Generation

In Figure 10, we see a rather complicated clocking and LO generation. Some of this complication is necessity and some is related to reuse of prior designs.

The 102.5 GHz LO is generated by doubling 51.25 GHz. 51.25 GHz is obtained by mixing 31.25 GHz and 20 GHz (10 GHz system clock multiplied by 2) and 31.25 GHz is generated by mixing 30 GHz and 1.25 GHz. 30 GHz is obtained by multiplying 5 GHz MSH clock output by 6 and 1.25 GHz is obtained by dividing 5 GHz MSH clock by 4 and a copy of the 1.25 GHz is fed back to the channel for phase locking the 102.5 GHz LO to the system phase reference. At startup, the 1.25 GHz signal comes up randomly with one of the four phases of 0° , 90° , 180° and 270° with respect to the system phase and during calibration of the system one of the phases is appropriately chosen and the absolute calibration phase value is stored. During normal startup the divider is reset

²Teledyne LeCroy scopes have eight major divisions vertically. Scopes generally have eight or ten

repeatedly until the phase of the 1.25 GHz is the same as the stored value of the phase.

The phase of the LO drifts over temperature because of high frequency mixing and multiplying and this needs to be compensated for, otherwise this will result in the phase of the HF/MF band to be shifted with respect to the phase of the LF band. To compensate for the LO phase drift, three coherent tones of 20.5 GHz, 41 GHz (20.5 GHz times two) and 82 GHz (41 GHz times two) are injected into the LF, MF and HF bands, respectively and this coherency is maintained throughout the operating temperature by adjusting the phase of the respective MF and HF band digital LO synthesizer. During the calibration, the reference phase shift between the 41 GHz and 20.5 GHz and 82 GHz calibration tones and the 20.5 GHz reference calibration tone is measured and stored during normal operation. Whenever the system detects a change in temperature, the user input is isolated and these coherent calibration tones are switched on and the phase difference between them is re-measured and the LO phase drift is recalibrated. The multipliers that generate the calibration tones are ovenized to maintain the coherency over temperature. A temperature sensor is also installed in the oven to monitor the temperature and can also be used to apply a secondary correction to correct for the phase drift of the tones.

VI. DIGITAL SIGNAL PROCESSING

Once the down converted signals, along with the LF base-band signals are acquired by the three 80 GS/s digitizers and stored in high-speed memory, the waveforms are read out and processed through the DSP processing as shown in Figure 11. All signals undergo an interleave correction filter, an adaptor, upsampler and fractional delay filter. The interleave correction removes the spurious response due to mismatched ADCs. The adaptor handles integer sample propagation time differences and the fractional delay handles the fractional sample time differences. The path propagation time differences are calibrated and stored in the instrument during factory calibration. The upsampler is required because mixing of the signal will cause images that, if not upsampled, will alias into bands of interest. The low image filter is used to define the image of interest after upsampling and before mixing is performed. The mixing action is performed between the LO and the signal from the low image filters. First the LO phase is determined. Because the system sample clock and the LO generation are locked together, the LO phase is a function of location within the acquisition memory. Once the phase is recovered, the digital LO is generated presumably in phase with the actual LO (but at least phase locked). The high image filters keep only the desired image. Sometimes, a crossover phase correction is employed to ensure that all bands sum constructively and holes do not appear in the response [11]. Prior to summing the band signals, a gain adjustment is applied to rescale the signals onto the same vertical scale and the waveforms are summed. The resultant signal is then compensated, first in magnitude, then in phase to produce the 100 GHz, 240 GS/s waveform acquisition.

The DSP processing system utilizes server class Intel® Xeon® X5660 processors (2.8 GHz per core, six cores per

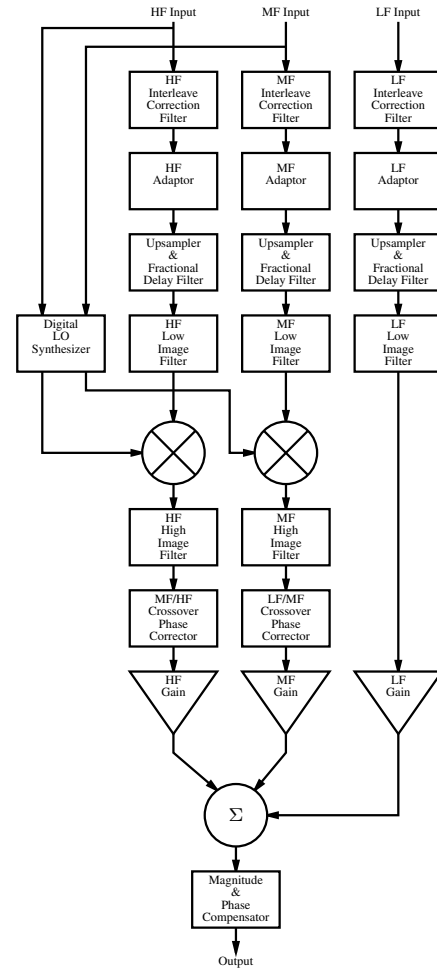


Figure 11. DSP Block Diagram

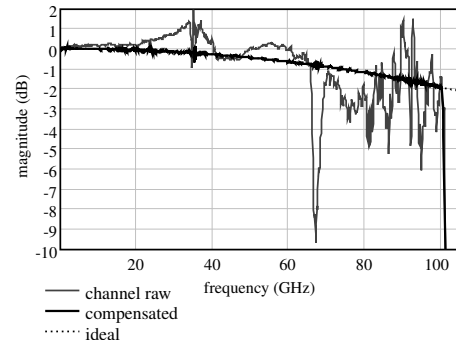


Figure 12. Magnitude Compensation

processor, and two processors for a 33.6 GHz total effective clock speed with up to 192 GB of RAM. Using Intel performance libraries, it can theoretically sustain calculation rates of about 100 GFLOPS. At approximately 20,000 FLOPs per sample point, the system achieves approximately 5 Mpoint/s throughput.

One of the most important elements in the DSP processing system is the magnitude and phase compensation system. The uncompensated magnitude response of the complete system is shown in Figure 12. Note that there are large variations in the

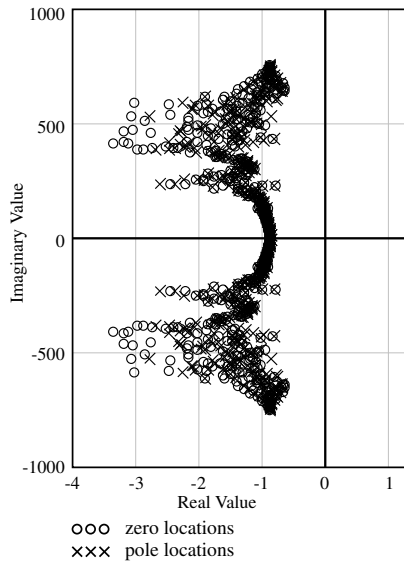


Figure 13. Pole Zero Locations of Magnitude Compensator

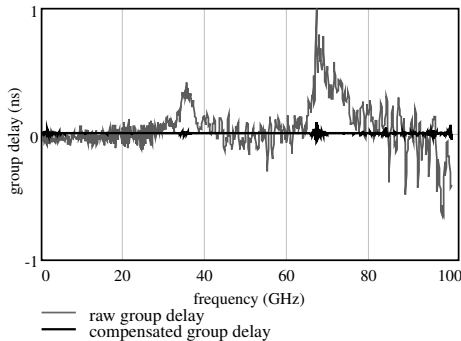


Figure 14. Group Delay Compensation

cross-over regions - the regions where the LF and MF intersect and where MF and HF intersect. During factory calibration, the delay of each path is adjusted so that the response in the cross-over region is maximized. As seen in Figure 12, the cross-over region between LF and MF bands has response much close to 0 dB. The high and the low peaks are to be expected since the phase may not add up constructively for the entire region. The cross-over region between MF and HF band shows a response that is 10 dB down. One of the reasons for such a response is that the response of the RF deck rolls off sharply in this region and hence adjusting the delay doesn't help much. In practice we do not want to have such a drop in the response because the filter has to boost the signal by 10 dB to make the final response close to 0 dB. Such an amplification will also boost the spurs in the region leading to incorrect behavior. Along the same lines, we do not want the raw response to have a peak greater than 3 dB either. A peak in the raw response indicates an amplification of the acquired analog signal. This amplification can increase the level of the analog signal, and this can saturate the ADCs leading to clipping of the waveform. In any case, the data shown is for a prototype unit and this dip in the raw response is being fixed in a future version.

More common raw responses are within -6 dB and 2 dB, and the filters are calculated so that the final response is a smooth one as shown in Figure 12. To correct the raw response an infinite impulse response (IIR) compensation filter [12] is designed using pole/zero fitting. For the raw response shown in Figure 12, up to 500 poles and zeros are used to generate the IIR filter with desired response. These analog pole and zero locations³ are plotted in Figure 13 where we see the large numbers of poles and zeros, many of them almost overlapping. They are fitted using techniques involving the Levenberg-Marquardt algorithm [13]. The original guess at the pole and zero locations fall onto a line of equal bandwidth close in to the $j\omega$ axis and restrictions are placed on how close they are allowed to get to the $j\omega$ axis to control inter-point behavior. The compensated response is shown overlaid with the raw response in Figure 12 where we see a nearly perfect fourth-order Bessel response with -2 dB⁴ attenuation at 100 GHz.

The phase or group delay compensation is as important as the magnitude compensation as the phase mostly determines the goodness of the step response and other time-domain oscilloscope characteristics. The raw group delay of the system (after magnitude response correction) is shown in Figure 14. As can be seen, the delay in the cross-over region between MF and HF is almost 1 ns. Such a group delay would cause the step response to be completely distorted.

We always compensate the group delay after the magnitude response. This is because the magnitude response is compensated with poles and zeros that also affect the phase response. The phase response is compensated with poles and zeros in an all-pass filter arrangement. All-pass filters are combinations of left half plane poles and right half plane zeros that affect the phase response but have no effect on the magnitude response. The filters are fit with a fuzzy logic grading system based on the step response as phase is an unreliable target for a fit [14]. For DBI, direct all-zero FIR filter design techniques are employed [15].

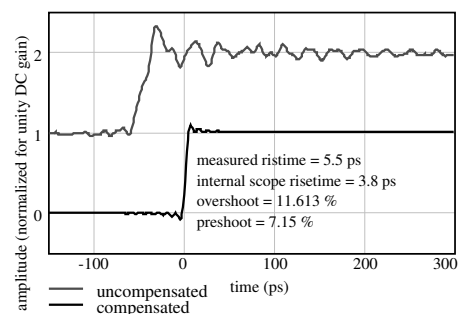


Figure 15. Uncompensated and Compensated Step Response

The step response with corrected and uncorrected group

³These locations are approximate as they are derived from digital filter pole and zero locations that line up on a rim on the unit circle in the z -domain. They are shown in the analog domain using the fact that $z = e^{\frac{s}{F_s}}$ which implies $s = \ln(z) \cdot F_s$. They are shown in the analog domain to gain insight into the analog behavior this filter is correcting.

⁴In oscilloscopes, we set the goal for the scope bandwidth point at -2 dB to provide 1 dB of margin to hopefully guarantee that the scope bandwidth specification is held in between calibration periods.

delay is shown in Figure 15. The group delay correction causes the system to be linear phase and provides for a step response rise time of about 4 ps.⁵ Teledyne LeCroy scopes offer programmable responses in three flavors: eye-diagram mode (Bessel roll-off and linear phase), flat (flat response and linear phase) and pulse-response (Bessel roll-off and minimum phase[16]).

VII. PERFORMANCE

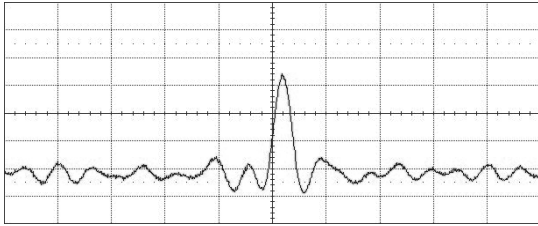


Figure 16. Optical Impulse Response

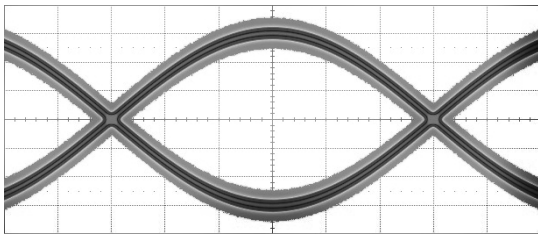


Figure 17. Eye Diagram

To demonstrate the performance of our 100 GHz oscilloscope employing all of the technology discussed thus far, consider two oscilloscope screens showing first, an optical impulse response in Figure 16 and an eye diagram shown in Figure 17⁶. In Figure 16, the impulse is displayed at 20 ps per division, so the pulse width is about 10 ps for a 5 ps rise and fall time. Based on other measurements we've performed with sampling oscilloscopes, this is the actual rise/fall time of this pulse, so the speed limit of the oscilloscope did not actually come into play. The trace was averaged to reduce noise.

In Figure 17, we have an eye pattern formed by our serial data analysis software on an acquired sinewave of 98.96 GHz according to the oscilloscope. It is displayed at 840 fs per horizontal division. The jitter measured is 63 fs random jitter with 20.1 fs deterministic jitter. This shows not only the vertical quality of the oscilloscope but also the quality of the oscilloscope timebase as well.

⁵The general rule of thumb for scopes is that the risetime multiplied by the bandwidth is a constant between 0.35 and 0.45 - 0.35 is for a single-pole rolloff and 0.45 would be for a steep (multi-pole) rolloff. High-end real-time scopes generally have very steep rolloffs.

⁶Normally, for oscilloscope performance, one wants to show screenshots of pseudo-random bit sequence (PRBS) waveforms and step response, but step and optical PRBS generators of sufficient quality and speed to properly show the oscilloscope performance were not available at the time this paper was written.

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